Submitted to ADVANCED MATERIALS

DOI: 10.1002/adfm.((please add manuscript number))

Thermal Properties of Nanostructured Electrodes for Phase Change Memory Devices

By Elah Bozorg-Grayeli*, John P. Reifenberg, Matthew Panzer, Jeremy A. Rowlette, and Kenneth E. Goodson

[*] Elah Bozorg-Grayeli
Stanford University, Bldg 530, Room 101
Stanford, CA, 94305 (USA)
E-mail: ((ebozorgg@stanford.edu))
Dr. J. P. Reifenberg
Intel Corporation
Santa Clara, CA, 95054
Dr. M. Panzer
KLA-Tencor
Milpitas, CA, 95035
Dr. J. A. Rowlette
Daylight Solutions
San Diego, CA, 92128
Dr. K. E. Goodson
Stanford University, Bldg 530, Room 214
Stanford, CA, 94305 (USA)

Keywords: Data Storage, Electrodes, Metals, Thin Films

Abstract – The switching current for phase change memory devices, which is a key figure of merit for this technology, can be strongly influenced by heat conduction in the electrodes. Here we propose and characterize a novel multilayer electrode stack, which uses series thermal boundary resistances to impede heat loss from the memory cell. Picosecond time-domain thermoreflectance captures the temperature-dependent thermal resistance of as-deposited and post-annealed single and multi-layer stacks based on carbon, titanium nitride, and tungsten nitride. The total thermal resistance of the W-WN_x stack decreases from 3.9 to 3.6 m^2 K GW^{-1} with annealing due to the reduction of interfacial defects. In contrast, the total thermal resistance of the C-TiN stack increases after annealing from 4.9 to 11.9 m^2 K GW^{-1}, likely due to interfacial mixing and disorder. The largest resistances reported here are equivalent to electrode films with thicknesses on the order of tens of nanometers.

Report Documentation Page

Form Approved
OMB No. 0704-0188

Public reporting burden for the collection of information is estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden, to Washington Headquarters Services, Directorate for Information Operations and Reports, 1215 Jefferson Davis Highway, Suite 1204, Arlington VA 22202-4302. Respondents should be aware that notwithstanding any other provision of law, no person shall be subject to a penalty for failing to comply with a collection of information if it does not display a currently valid OMB control number.

1. REPORT DATE	2. REPORT TYPE	3. DATES COVERED
2011		**00-00-2011 to 00-00-2011**

4. TITLE AND SUBTITLE	5a. CONTRACT NUMBER
Thermal Properties of Nanostructured Electrodes for Phase Change Memory Devices	5b. GRANT NUMBER
	5c. PROGRAM ELEMENT NUMBER
6. AUTHOR(S)	5d. PROJECT NUMBER
	5e. TASK NUMBER
	5f. WORK UNIT NUMBER
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) **Stanford University,Bldg 530, Room 101,Stanford,CA,94305**	8. PERFORMING ORGANIZATION REPORT NUMBER
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)	10. SPONSOR/MONITOR'S ACRONYM(S)
	11. SPONSOR/MONITOR'S REPORT NUMBER(S)

12. DISTRIBUTION/AVAILABILITY STATEMENT
Approved for public release; distribution unlimited

13. SUPPLEMENTARY NOTES

14. ABSTRACT

The switching current for phase change memory devices, which is a key figure of merit for this technology, can be strongly influenced by heat conduction in the electrodes. Here we propose and characterize a novel multilayer electrode stack, which uses series thermal boundary resistances to impede heat loss from the memory cell. Picosecond timedomain thermoreflectance captures the temperature-dependent thermal resistance of asdeposited and post-annealed single and multi-layer stacks based on carbon, titanium nitride and tungsten nitride. The total thermal resistance of the W-WNx stack decreases from 3.9 to 3.6 m2 K GW-1 with annealing due to the reduction of interfacial defects. In contrast, the total thermal resistance of the C-TiN stack increases after annealing from 4.9 to 11.9 m2 K GW-1 likely due to interfacial mixing and disorder. The largest resistances reported here are equivalent to electrode films with thicknesses on the order of tens of nanometers.

15. SUBJECT TERMS

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE			
unclassified	**unclassified**	**unclassified**	**Same as Report (SAR)**	**10**	

Introduction

Reducing the energy consumption during switching is a key challenge for the competitiveness of phase change memory technologies.[1] The switching behavior of a phase-change memory (PCM) cell depends on device size,[2] applied fields,[3] and the temperature gradient developed at the electrode-device interface.[2] The near electrode temperature gradient is governed by thermal conduction within and near the device. Reifenberg et al demonstrated through coupled electrical-thermal simulations that the programming current of a $Ge_2Sb_2Te_5$ (GST) based device decreases as the total thermal resistance of the cell increases.[2] Karpov and Kostylev showed that much of the heat generated during GST cell switching occurs in the GST bulk and at the electrode interface.[4] For this reason, one of the goals in PCM thermal design is to minimize heat loss from the cell. Since heat loss through the electrode dominates in many PCM cell geometries, electrode materials with low thermal conductivities and larger thermal boundary resistance (TBR) can therefore reduce heat loss in PCM cells. The TBR is a function of the acoustic properties in the adjacent materials and the presence of near-interfacial disorder.[5-6] Previous work shows data for GST-electrode TBR in the range of 5 to 50 $m^2K\ GW^{-1}$.[7-8] However, as shown in,[7] electrodes with low thermal conductivities may not have high TBR. For electrode materials such as C, Ti, and TiN, the thermal boundary resistance becomes comparable to intrinsic thermal resistance when the film thicknesses approaches ~ 30 nm. As such, there may not be a single composition electrode material which is suitable for use at multiple thickness scales. Therefore, designers must consider new ways to utilize the GST-electrode TBR while increasing the intrinsic electrode thermal resistance. Multilayer electrode stacks offer a way to achieve this.

In order to minimize the heat loss from a GST cell, we propose here a multilayer electrode stack (**Fig. 1**). The presence of the material interfaces in these electrodes would contribute significantly to the total thermal resistance of the stack. Further, the bottom film of the stack can be chosen to maximize the GST-electrode TBR, which impedes heat loss from the PCM

cell and reduces the programming current.[2] This paper measures and assesses the importance of TBR in three prospective PCM electrode materials. Samples are measured as-deposited and after a 5 minute anneal at 400 ^{o}C. A picosecond thermoreflectance setup interrogates the thermal properties of the samples in an optical access oven. Multilayer stacks of electrode materials are measured to determine the electrode-electrode TBR for C-TiN and W-WN. Temperature-dependent measurements of all samples determines thermal conductivity and TBR in the range of 25 to 400 ^{o} C.

Experimental Method

A picosecond Time-Domain Thermoreflectance (TDTR) setup extracts the thermal properties of these materials. TDTR is a well-established optical measurement technique that uses delayed pump and probe laser pulses to heat a sample and interrogate its temperature response [9-10]. Since metals exhibit linear changes in reflectivity with temperature for small temperature changes, this technique extracts a normalized temperature decay for a heated metal transducer film on a stack of thin film materials [11].

In this setup, a 9.2 ps, 1064 nm, passively-modelocked Nd:YVO_4 laser with 82 MHz repetition rate acts as the pump and probe source. A waveplate-beamsplitter pair controls the ratio of pump to probe power. The probe component is delayed from the pump via a variable delay stage, allowing data collection from -200 ps to 3500 ps relative to the peak of the thermoreflectance trace. An optical access oven controls the temperature of the sample from 30 to 400 ^{o}C. The oven maintains a vacuum to prevent transducer oxidation.

The Feldman Algorithm for heat flow through a multilayer stack fits the decay curves [12-13]. The model considers 3-D rotationally symmetric heat deposition at the transducer-ambient interface. The intrinsic electrode thermal conductivity, transducer-electrode TBR, and electrode-silicon TBR are used as fitting parameters.

All samples were deposited using magnetron sputtering. Tungsten deposition utilized DC power and argon plasma. Carbon deposition used pulsed-DC power at 90 kHz with argon

plasma. TiN and WN were both deposited using DC power and reactive argon-nitrogen plasma with, respectively, pure titanium and pure tungsten sputtering targets. The multilayer samples underwent similar deposition, without air breaks in the C-TiN or W-WN layers. Single-layer samples of each film ranged in thickness from 25 – 100 nm. The multilayer stacks consisted of 5 periods of W/WN (70 nm/100 nm) or C/TiN (11 nm/110 nm). A 50 nm aluminum layer acts as the transducer for each sample. Annealed samples were held for 5 minutes at 400 ^{o}C, with ramp-up taking less that 60 minutes and cool down taking less than 30 minutes.

For the film compositions in this work, and at times scales below ~400 ps, the thermal decay time of the transducer layer is dependent on the heat capacitance of the film and the Al-electrode TBR, such that at short times, $\tau \sim R_{Al\text{-}elec}C_{Al}$. During this time period, the thermal decay behavior is sensitive to only the transducer-electrode TBR. As a result, the TBR is uniquely separable from the electrode thermal conductivity [8]. For the multilayer samples, the model fits an effective thermal resistance for each individual electrode layer. For the W-WN sample, this becomes an effective thermal conductivity for each electrode material type. The total thermal resistance of a W-WN pair is calculated, and the intrinsic thermal resistances of the WN and W layers are subtracted out, leaving a resistance equal to twice the W-WN TBR. For W, the intrinsic conductivity is obtained by scaling the bulk conductivity to account for boundary scattering. For the C-TiN sample, since the carbon layers are very thin, the model treats the stack as several layers of TiN with equal TBR between each layer. This TBR term includes the intrinsic carbon resistance and the C-TiN TBR. Subtracting out the intrinsic C thermal resistance leaves a resistance equal to twice the C-TiN TBR.

Results and Discussion

All single-layer samples exhibit a decrease in total thermal resistance ($R_{total}=L_{electrode}/k_{electrode} + R_{Al\text{-}electrode} + R_{electrode\text{-}si}$) as temperature rises, with the as-deposited samples showing significant temperature hysteresis. After separating out the TBR terms from the total

resistance, only the titanium nitride sample shows an increase in intrinsic thermal conductivity after annealing (**Fig. 2**). This may be due to a decrease in defect density within the TiN film, resulting in a higher phonon mean free path. In all other cases, the thermal resistance decreases due to annealing of the material interfaces. Conducting the same measurement on the annealed samples demonstrates the hysteresis effect is no longer visible. This indicates that the five minute anneal time is sufficient to promote temperature stability of single-layer electrode thermal properties. The data shown in figure 2, form the fitting parameters for the multilayer stacks. Error due to signal noise is small. As a result, thickness uncertainty dominates the error bars.

The single-layer carbon films demonstrate similar thermal conductivity to amorphous carbon films measured by Bullen et al.[14] It has been reported that annealing amorphous carbon films at temperature greater than ~ 400 ^{o}C results in the formation of crystalline structures.[15] Thermal conductivity measurements of graphitic structures show in plane conductivity to be ~300 times as high as cross plane conductivity.[16] The experimental parameters here render the measurement insensitive to the lateral thermal properties of the carbon. In order to observe this effect using TDTR, the setup requires thicker carbon films, thinner pump waist, or lower modulation frequency.

Both annealing time and temperature impact the thermal conductivity of the TiN and WN films. Annealing these samples before conducting high temperature measurements results in a higher thermal conductivity at 400 ^{o} C than for the as-deposited films. This may be due to the annealed samples spending a greater total amount of time at elevated temperature. As a result, the annealed samples would have a lower dislocation density than the as-deposited samples, resulting in a higher thermal conductivity.

For the multilayer stacks, W-WN exhibited a small decrease in thermal boundary resistance due to annealing, from 3.9 $m^2K\ GW^{-1}$ to 3.6 $m^2K\ GW^{-1}$ (**Fig. 3**). The annealed sample showed no temperature hysteresis. The C-TiN multilayer, on the other hand, showed a significant

increase in the apparent TBR after annealing, from 4.9 $m^2K\ GW^{-1}$ to 11.9 $m^2K\ GW^{-1}$. Since the carbon layers were roughly 10 nm thick, interdiffusion from the TiN layers at high temperature may have resulted in a highly disordered film rather than a solid interface.[17] Interdiffusion in this disordered layer would significantly decrease the phonon mean free path due to impurity scattering, resulting in a lower thermal conductivity. The measured thermal conductivity is therefore representative of an elementally heterogeneous film. The absence of a sharp material interface in this film implies the need for careful interpretation of the extracted TBR. For this reason, figure 3 defines an apparent TBR using the intrinsic carbon thermal conductivity determined from the single layer samples.

Using the data obtained above, an estimate of the electrical resistivity of the multilayer stacks is available. Using the Wiedemann-Franz-Lorenz (WFL) law, the electrical conductivity of a metal at temperatures on the order of its Debye temperature can be estimated from its thermal conductivity, the temperature, and the Lorenz coefficient. Since the WN and TiN electrodes are metallic in nature, WFL provides an estimate of the resistivity of the two films. The data shown in figures 2 and 3 give a TiN resistivity of ~ 100 μΩ-cm, and a WN resistivity of ~ 150 μΩ-cm. In comparison, the estimated resistivity of the tungsten layer, based on scaling the bulk conductivity due to the presence of material boundaries, is ~ 10 μΩ-cm. It would be inappropriate to use this method for the carbon film, as thermal conduction is phonon dominated. Further, since WFL functions for material interfaces as well as bulk materials, the multilayer electrical resistivity may also be estimated.[18] For the W-WN stack, this becomes ~ 120 μΩ-cm, and for the C- TiN stack, this becomes ~ 270 μΩ-cm.

Conclusions

This letter introduces a novel nanostructured multilayer electrode stack that exhibits significant increases in thermal resistance relative to single material electrodes. This additional resistance can reduce the programming current in many PCM cell geometries. Specifically, C-TiN electrode stacks offer both high intrinsic resistance and high thermal

boundary resistance. Annealing gives control over the thermal resistances of the PCM cell. It may also lead to further incorporation of titanium and nitrogen into the carbon layer. This makes it difficult to define a solid material interface. As such, the results presented here define an apparent boundary resistance based on the anticipated intrinsic thermal resistance of the carbon layer.

Acknowledgments

The authors would like to thank Kuo-Wei Chang and his colleagues at Intel Corporation for their assistance on this paper. Thanks are also due to Enrico Varesi, Davide Erbetta, and Roberto Bez for sample preparation and editting assistance. This research was made with Government support under and awarded by DoD, Air Force Office of Scientific Research, National Defense Science and Engineering Graduate (NDSEG) Fellowship, 32 CFR 168a.

Received: ((will be filled in by the editorial staff))
Revised: ((will be filled in by the editorial staff))
Published online: ((will be filled in by the editorial staff))

_[1] H. S. P. Wong, S. Raoux, S. B. Kim, J. Liang, J. P. Reifenberg, B. Rajendran, M. Asheghi, and K. E. Goodson, *Proc. of the IEEE,* **2010**, *98*, 12.

_[2] J. P. Reifenberg, D. L. Kencke, and K. E. Goodson, *IEEE Elec. Dev. Lett.*, **2008**, *29*, 10.

_[3] K. Homma, H. K. Henisch, and S. R. Ovshinsky, *Jour. of Non-Crys. Sol.*, **1980**, *35 & 36*.

_[4] I. V. Karpov and S. A. Kostylev, *IEEE Elec. Dev. Lett.*, **2006**, *27*, 10.

_[5] I. M. Khalatnikov and I. N. Adamenko, *Sov. Phys. JETP*, **1973**, *36*.

_[6] E. T. Swartz and R. O. Pohl, *Rev. of Mod. Phys.*, **1989**, *61*, 3.

_[7] E. Bozorg-Grayeli, J. P. Reifenberg, K. W. Chang, M. Panzer, and K. E. Goodson, in *ITHERM 2010*, Las Vegas, **2010**.

_[8] J. P. Reifenberg, K. W. Chang, M. Panzer, S. B. Kim, J. A. Rowlette, M. Asheghi, H. S. P. Wong, and K. E. Goodson, *IEEE Elec. Dev. Lett.*, **2010**, *31*, 1.

_[9] M. A. Panzer, M. Shandalove, J. A. Rowlette, Y. Oshima, Y. W. Chen, P. C. McIntyre, and K. E. Goodson, *IEEE Elec. Dev. Lett.*, **2009**, *30*, 12.

_[10] J. Rowlette, R. Kekatpure, M. A. Panzer, M. Brongersma, and K. E. Goodson, *Phys. Rev. B*, **2009**, *80*, 4.

_[11] K. Ujihara, *IEEE Jour. of Quant. Mech.*, **1972**, *8*, 6.

_[12] A. Feldman, *High Temp – High Pres.*, **1999**, *31*, 3.

_[13] D. G. Cahill, *Rev. Sci. Instrum.*, **2004**, 75, 12.

_[14] A. J. Bullen, K. E. O'Hara, D. G. Cahill, O. Monteiro, and A. von Keudell, *Jour. of App. Phys.*, **2000**, *88*, 11.

_[15] R. O. Dillon, J. A. Woollam, and V. Katkanant, *Phys. Rev. B*, **1984**, *29*, 6.

_[16] A. J. Schmidt, *Optical Characterization of Thermal Transport from the Nanoscale to the Macroscale (Thesis)*, MIT, Boston, USA, **2008**.

_[17] T. Beechem and P. E. Hopkins, *Jour. of App. Phys.*, **2009**, *18*, 12.

_[18] G. D. Mahan and M. Bartkowiak, *App. Phys. Lett.*, **1999**, *74*, 7.

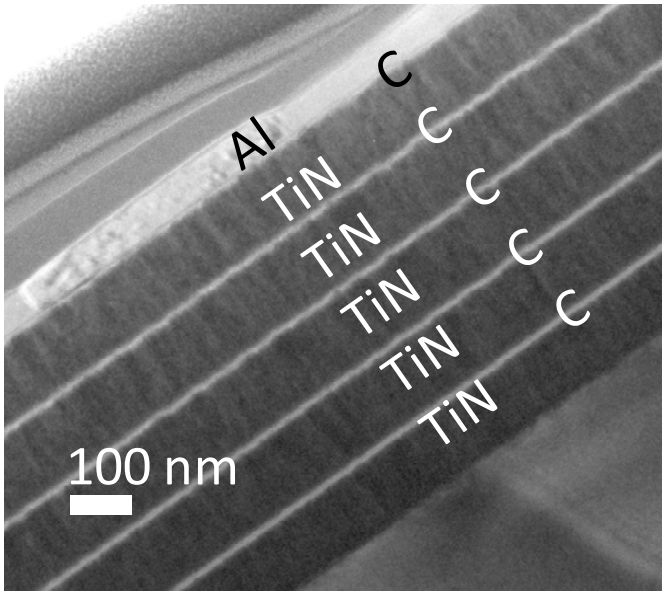

Figure 1. Cross-sectional TEM image of the C-TiN multilayer electrode stack with the Al transducer on top.

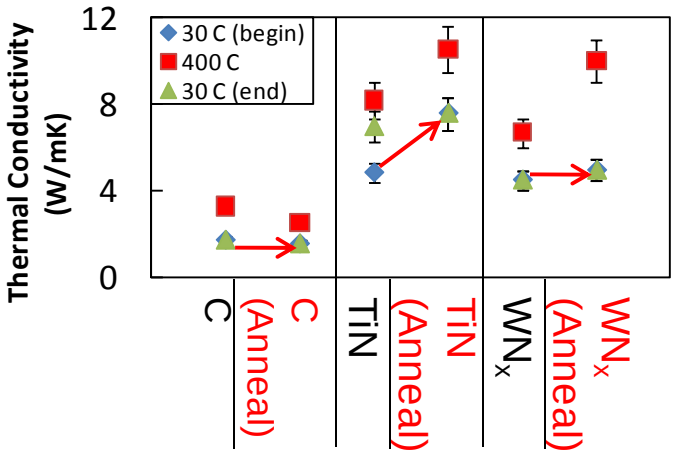

Figure 2. Thermal conductivity of the single-layer electrode samples. The red arrows indicate the change of room temperature conductivity between the as-deposited and post-annealed samples. Error bars are due to uncertainty in sample thickness.

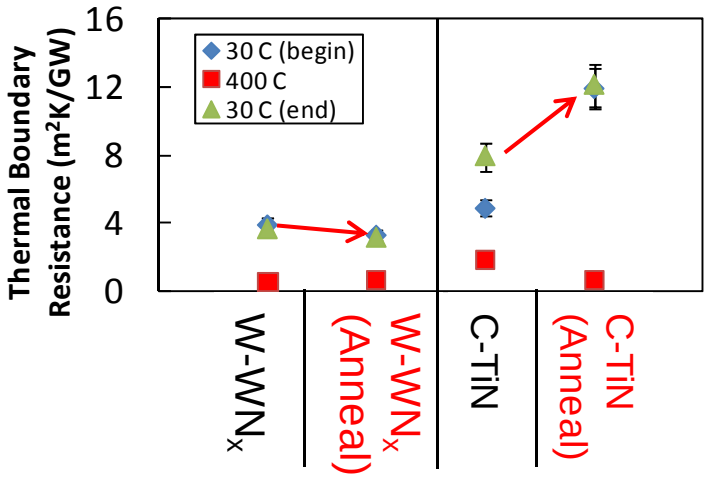

Figure 4. Thermal boundary resistance electrode multilayer samples. The red arrows indicate the change of room temperature TBR between the as-deposited and post-annealed samples. Error bars are due to uncertainty in the thickness of the electrode films.

The table of contents entry: The thermal properties of phase change random access memory (PCRAM) devices significantly affect their switching behavior. This paper demonstrates a novel, nanostructured electrode material that improves upon existing PCRAM electrodes. The presence of multiple material interfaces impedes heat loss from the memory cell, allowing it to switch with lower input current.

Keyword: Electrodes

Elah Bozorg-Grayeli*, John P. Reifenberg, Matthew Panzer, Jeremy A. Rowlette, and Kenneth E. Goodson

Title **Thermal Properties of Nanostructured Electrodes for Phase Change Memory Devices**

ToC figure